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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PATEL, CHIRAG R	

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/084,474	MACIEL, FREDERICO BUCHHOLZ	
	Examiner	Art Unit	
	Chirag R. Patel	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 2001-361913.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Albert et al. (US 6,891,839).

As per claims 1, 5, 8 and 10, Albert et al. discloses an information processing system to be accessed through a network, comprising: a plurality of information processors for executing information processing in response to a received packet; (Col 7 lines 25-35,Figure 2A items 231-232, 241-242)

a plurality of address translators capable of operating in parallel with each other and being disposed between an external network and an internal network to which said

information processors are connected, (Col 7 lines 35-40, Col 9 lines 5-8, Col 10 lines 33-37, Col 15 lines 60-65, Figure 2A items 241-242)

each of said address translators operating to translate a destination address of a packet received from said external network to an address indicative of one of said information processors to be accessed, and to transfer the address-translated packet to said internal network; (Col 12 lines 30-36, Col 15 lines 60-65)

means for holding an access correspondence table corresponding to each of said address translators, (Col 10 lines 25-29, Figure 2B item 254)

said access correspondence table having a plurality of control information entries each defining the relation among a source address, an address assigned to an external interface connected to said external network, and a destination address indicative of an information processor to be accessed; (Col 8 lines 21-35, Col 17 lines 55-65, Figure 7)

and a controller for switching an access route to a specific information processor from a first route passing through a first address translator to a second route passing through a second address translator, (Col 11 lines 17-27)

said controller having means for instructing said second address translator to store received packets for accessing said specific information processor into a memory, (Col 11 lines 17-27, Figure 2C item 282, Figure 2C item 274)

instructing said first and second address translators to change address information, which is set to designate packets to be received, in such a manner that the packets for accessing said specific information processor are received by the second address translator in place of said first address translator, (Col 11 lines 17-27)

shifting a control information entry whose destination address indicates said specific information processor from an access correspondence table corresponding to said first address translator to an access correspondence table corresponding to the second address translator, (Col 9 lines 19-32) and

notifying said second address translator of end of the route switching, and wherein said second address translator starts, in response to said notification of end, an operation of translating the destination address of packets stored in said memory in accordance with said access correspondence table corresponding to the second address translator to transfer the packet to said internal network. (Col 14 lines 58-67, Col 15 lines 1-4)

As per claim 2, Albert et al. discloses the information processing system according to claim 1, wherein said controller composes a part of one of said plurality of information processors. (Col 11 lines 17-19, Figure 2C item 282)

As per claim 3, Albert et al. discloses the information processing system according to claim 1, wherein each of control information entries registered in each of said access correspondence tables includes an internal address assigned to an internal interface connected to said internal network in correspondence with an information processor to be accessed, and (Col 17 lines 55-65,Col 33 lines 52-57, Figure 7 item 712)

each of said address translators translates a destination address and a source address of a packet received from said external network into a destination address and an internal address indicated by one of control information entries in an access correspondence table corresponding to the address translator. (Col 14 lines 1-7)

As per claim 4, Albert et al. discloses the information processing system according to claim 1,

wherein each of said address translators has an access correspondence table corresponding thereto, a copy of each of control information entries in each of said access correspondence tables is stored in one of said information processors corresponding to a destination address defined in the control information entry, and (Col 11 lines 17-27, Col 9 lines 19-25, Col 17 lines 55-65, Figure 7 item 712)

said controller performs said shifting of said control information for switching the access route by using the copy. (Col 9 lines 26-32)

As per claim 6, Albert et al. discloses a packet processing method in an address translator for translating an address of a packet received from an external network and transferring the packet to an internal network to which a plurality of information processors are connected, (Col 12 lines 30-36, Col 15 lines 60-65) comprising the steps of:

when a control packet for starting an access to one of said information processors is received from said external network, generating a control information

entry indicative of a corresponding relation among an address of a packet transmission source, an address assigned to an external interface which has received said control packet, and a destination address indicative of one of said information processors to be accessed, (Col 8 lines 21-35, Col 17 lines 55-65, Figure 7)

and registering the control information entry into an access correspondence table; (Col 20 lines 63-67)

when a message indicating that an access route with respect to an address assigned to said external interface is being switched is received from a controller connected to said internal network, registering said address in a memory as an address in a transition mode; (Col 7 lines 40-53, Col 9 lines 19-32, Col 15 lines 60-65, Col 20 lines 63-67, Col 21 lines 1-9, Figure 2C item 274)

when a user packet is received from said external network, (Col 10 lines 41-43, Col 15 lines 60-65)

referring to said access correspondence table and, if a control information entry corresponding to the received packet is registered, (Col 20 lines 63-67, Col 21 lines 1-9, Figure 9A item 906)

translating a destination address of said received packet in accordance with the control information entry and transferring the address-translated packet to said internal network; and (Col 15 lines 30-37)

when the control information entry corresponding to said received packet is not registered in said access correspondence table, if the destination address of the received packet is registered as the address in said transition mode, storing the

received packet into a memory and, if the destination address of the received packet is not registered as the address in said transition mode, discarding the received packet. (Col 20 lines 63-67, Col 21 lines 1-9, Figure 2C item 274, Figure 9A item 906)

As per claim 7, Albert et al. discloses the packet processing method according to claim 6, further comprising the step of: saving the contents of each control information entry registered in said access correspondence table into an information processor indicated by a destination address of the entry at a predetermined timing. (Col 21 lines 37-45)

As per claim 9, Albert et al. discloses a method of shifting a packet transfer load according to claim 8, wherein each of said address translators has said control table to be referred to, (Col 17 lines 55-65, Figure 7) and the method further comprises the steps of:

storing in each of said information processors a copy of information entries each including an address of the information processor as a destination address; and (Col 11 lines 17-27, Col 11 lines 57-65, Figure 7 item 712)

shifting the control information entry held by said specific information processor to a control table to be referred to by said second address translator. (Col 9 lines 19-32, Col 11 lines 17-27)

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Albert et al. (US 6,704,278) discloses a system and method are disclosed for providing a fault tolerant network service. Wilson (US 6,718,347) discloses a method and apparatus for maintaining coherence among copies of a database shared by multiple computers. Gigliotti et al. (US 6,393,458) discloses a method and apparatus for load balancing in a distributed object architecture. Aiken JR. (US 2002/0143965) discloses establishing an affinity between a particular server application and a particular client in a computing network, where that network performs workload balancing. Hay (US 2002/0152322) discloses a method and apparatus for facilitating load balancing across name servers. Wolff (US 6,185,601) discloses dynamic load balancing of a network of client and server computers. Bachmat et al. (US 6,711,649) discloses load balancing on disk array storage device. Kremien (US 2001/0034752) discloses Method and system for symmetrically distributed adaptive matching of partners of mutual interest in a computer network.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag R. Patel whose telephone number is (571)272-7966. The examiner can normally be reached on Monday to Friday from 7:30AM to 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rupal Dharia, can be reached on (571) 272-3880. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER